

# Application Note 2007-001

## Configuring the DSK\_AUDIO4 Codecs for Master Mode Operation

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## 1 Background

The DSK\_AUDIO4 daughtercard is designed to synchronize the sampling of the two codecs by operating both codecs sharing the same CLKX/CLKR and FSX/FSR signals. On power-up or reset, the daughtercard initializes both codecs as slave devices. To operate in this configuration, McBSP1 is configured as the master and McBSP0 is configured as a slave. A master device generates the CLKX/CLKR and FSX/FSR signals, while a slave device accepts the CLKX/CLKR and FSX/FSR signals as inputs.

Alternatively, it is possible to configure codec 1 to operate as a master, and configure McBSP1 as a slave. In this case, codec 1 generates the CLKX/CLKR and FSX/FSR signals for both McBSPs and codec 0. This is described in detail in section 2.

A 74LVC2G34 dual buffer (U5) on the daughtercard is used to drive the CLKX1/FSX1 signals generated McBSP1 onto the CLKX0/FSX0 signals for McBSP0 and the attached PCM3794 codec 0 (U1). To prevent signal contention, **do NOT configure codec 0 or McBSP0 as master devices**. If you wish to operate U1 or McBSP0 as a master, then U5 must be removed from the board in order to isolate the McBSP1/0 CLKX and FSX signals. This is described in detail in section 3.

It is strongly recommended that before modifying any codec registers, you review in detail the PCM3794 datasheet and the file *pcm3793.h* used in the sample software projects.

## 2 Operating Codec 1 as Master

To operate codec 1 as a master, you must first determine the desired operating mode for the codec audio serial interface. (See the PCM3794 datasheet page 21-23.) The mode used in the example software is the DSP Format (Figure 28e). In this mode, it is still possible to obtain the left and right sample data in a single 32-bit word from the McBSP. This eliminates any issues with the left/right data losing synchronization when debugging. The software changes required to implement this change are actually quite minor.

1. Configure MCBSP1 and McBSP0 as slave devices.
  - a. The `Init_McBSP` function has been modified to support slave operation with the DSP Format. Note that in the DSP Format, the first data bit is delayed by one bit clock after the frame sync. To be compatible, the McBSP RCR register must be configured for `RDATDLY = 1`, and the McBSP XCR register must be configured for `XDATDLY = 1`.

```
port->rcr = 0x000500A0; // 1-phase, 32-bits, 1 bit data delay
port->xcr = 0x000500A0;
```

2. Configure codec 1 and codec 0 to use DSP Format.
  - a. Before configuring the codecs, it is recommended to force them back to their default condition. This ensures that they will be in a known condition if the program is ever restarted without resetting the daughtercard. Then, the ADC and DAC audio serial interface of the codecs can be set to DSP Format. Note that in both cases, the relevant codec registers contain additional settings that must be included. The settings shown match the default configuration of the codecs by the DSK\_AUDIO4 board. (At sample rates less than 24kHz, the DAC output signal can be improved by changing the *PCM3793\_REG\_DAC\_CNFIG* value to include *PCM3793\_REG\_DAC\_CNFIG\_OVER*.)

```
DskAudio4_ResetDaughterCardToDefaults();  
DskAudio4_WriteCodecSetting(0, PCM3793_REG_DAC_CNFIG,  
PCM3793_REG_DAC_CNFIG_DEM_OFF | PCM3793_REG_DAC_CNFIG_PFM_DSP); // codec 0 DAC  
DskAudio4_WriteCodecSetting(0, PCM3793_REG_ADC_CNFIG,  
PCM3793_REG_ADC_CNFIG_HPF_4HZ | PCM3793_REG_ADC_CNFIG_RFM_DSP); // codec 0 ADC  
DskAudio4_WriteCodecSetting(1, PCM3793_REG_DAC_CNFIG,  
PCM3793_REG_DAC_CNFIG_DEM_OFF | PCM3793_REG_DAC_CNFIG_PFM_DSP); // codec 1 DAC  
DskAudio4_WriteCodecSetting(1, PCM3793_REG_ADC_CNFIG,  
PCM3793_REG_ADC_CNFIG_HPF_4HZ | PCM3793_REG_ADC_CNFIG_RFM_DSP); // codec 1 ADC
```

3. Configure codec 1 as a master device.
  - a. Before setting codec 1 to master mode, the operating frequency must be set according to Table 11 of the PCM3794 datasheet. For the 12.288MHz master clock used on the daughtercard, there are a number of possible sample rates that can be obtained. The values for NPR and MSR that are specified for a given sample rate are then used to program the codec. The example code sets NPR=0 and MSR=2, for a sample rate of 48kHz. The codec mode can be set to master, which will cause it to begin generating the frame sync and bit clock signals that will be used by the McBSPs and codec 0. Note that *PCM3793\_REG\_MODE\_BIT0* must be specified for correct operation of the codec.

```
DskAudio4_WriteCodecSetting(1, PCM3793_REG_SYS_RESET, 0); // NPR[5:0]  
DskAudio4_WriteCodecSetting(1, PCM3793_REG_SYS_CNFIG,  
2 << PCM3793_REG_SYS_CNFIG_MSR_SHIFT); // MSR[2:0]  
DskAudio4_WriteCodecSetting(1, PCM3793_REG_MODE, PCM3793_REG_MODE_MASTER |  
PCM3793_REG_MODE_BIT0);
```

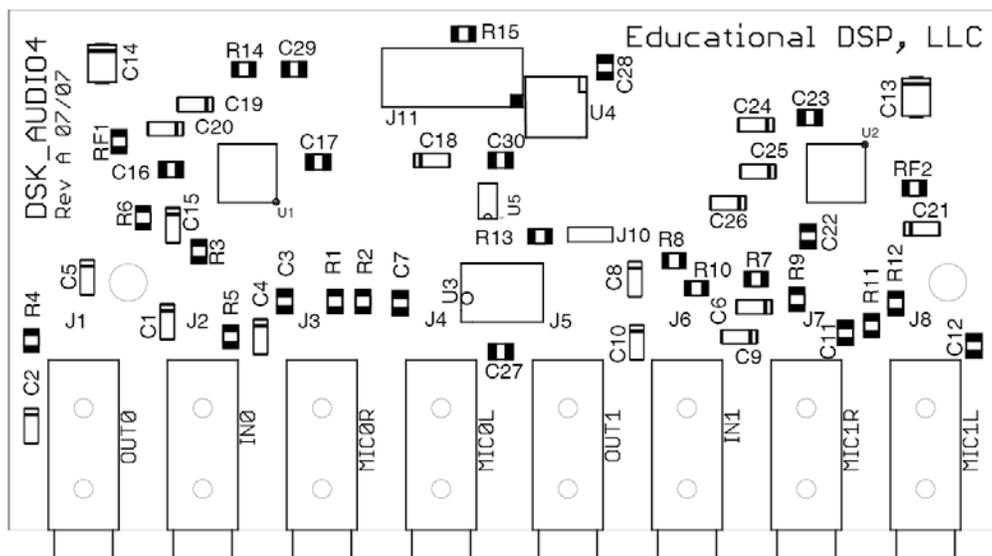
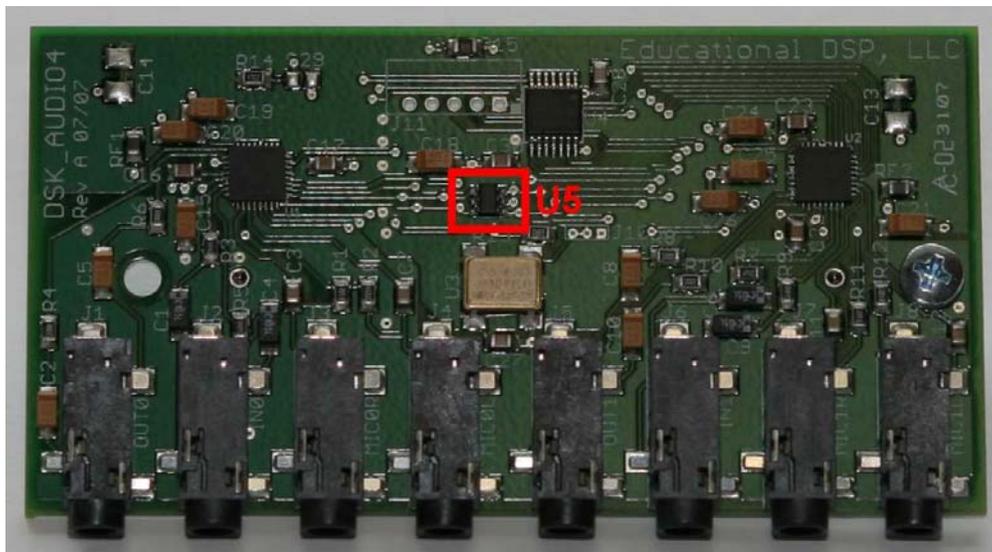
The sample software projects have all of the required code. In our experience, operating a PCM3794 as a slave codec at sample frequencies below 16kHz results in a degraded output signal, and is not recommended.

### 3 Operating Codec 1 & 0 as Masters

There are two primary reasons why it may be desirable to operate both codecs as masters;

- You want the codecs to operate at different sample rates, or,
- You want to operate both codecs at low samples (< 16kHz).

In order to operate both codecs as masters, the 74LVC2G34 dual buffer (U5) **must be removed**. The buffer is located on the board as shown below. Use proper removal tools and techniques to avoid damaging the board or other components when removing U5.



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Once U5 is removed, codec 0 can be safely configured as a master in the same manner as described previously for codec 1, as shown below. The two codecs can now be set to different sample rates, if desired.

```
DskAudio4_WriteCodecSetting(0, PCM3793_REG_SYS_RESET, 0); // NPR[5:0]
DskAudio4_WriteCodecSetting(0, PCM3793_REG_SYS_CNFIG,
    2 << PCM3793_REG_SYS_CNFIG_MSR_SHIFT); // MSR[2:0]
DskAudio4_WriteCodecSetting(0, PCM3793_REG_MODE, PCM3793_REG_MODE_MASTER |
    PCM3793_REG_MODE_BIT0);
```

Note that if the two codecs are operated at different sample rates, you must use separate interrupt service routines for McBSP0 and McBSP1. If the codecs are operated at the same sample rate, it is still possible to use a single interrupt service routine as done in the example software. In that case, you should ensure that codec 1 is started **after** codec 0, so that when the McBSP1 interrupt occurs the data has already been transmitted/received by McBSP0.