DSK_COMM4

Communications Daughtercard

for the

Texas Instruments

TMS320C6X11/6713/6416T/5510/5416

Digital Signal Processing (DSP) Starter Kits

(Board Revision B.1)

Educational DSP, LLC

www.educationaldsp.com

1 Hardware

1.1 Overview

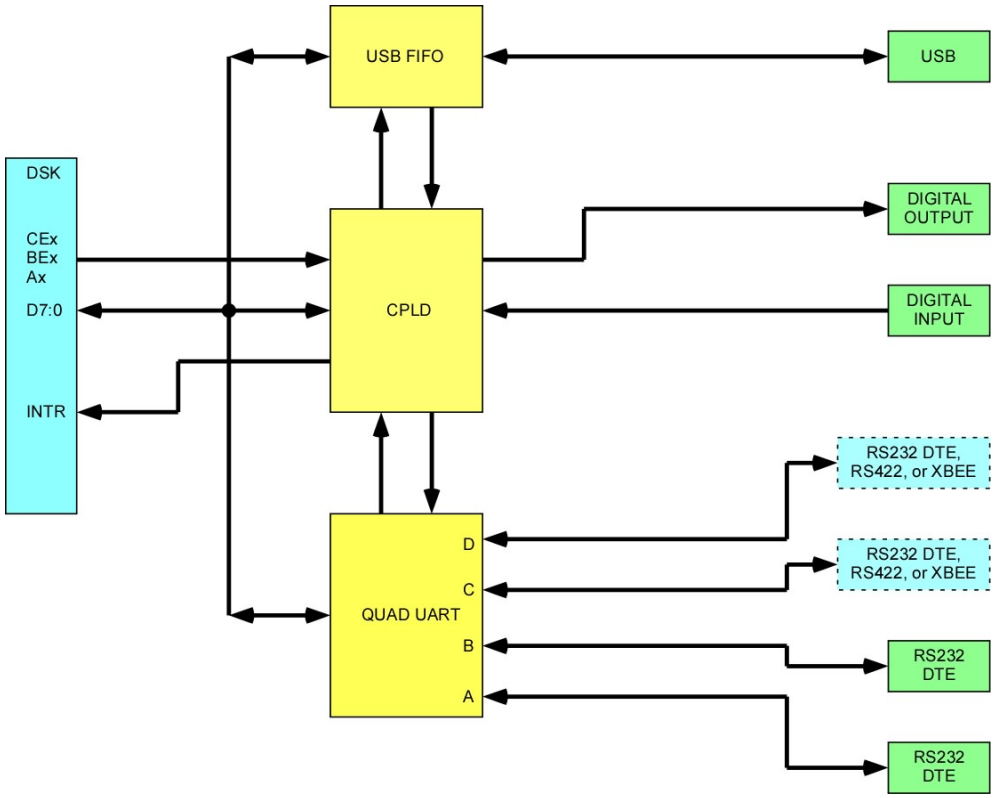
The DSK_COMM4 is a multichannel serial data input/output daughtercard designed to operate on the Texas Instruments TMS320C5416, TMS320VC5509A, TMS320VC5510, TMS320C6211, TMS320C6416T, TMS320C6711, and TMS320C6713 DSP Starter Kits (DSKs).

The basic daughtercard configuration contains a four-channel UART (TI TL16C554), a USB FIFO interface (FTDI FT245R), 8 pins of digital input, and 8 pins of digital output. Full RS-232 DTE serial interfaces are implemented on UART channels A and B. UART channels C and D are not used in the basic configuration, but can optionally be populated with any one of the following options;

- RS-232 full DTE interface
- RS-422 transceiver interface
- Digi (MaxSteam) XBee radio module supporting 802.15.4 protocol

The daughtercard can also be populated with pass-through connectors that allow stacking of daughtercards.

An overall block diagram of the daughtercard is shown below. More detailed information on the individual functions is available in the following sections.



1.2 General Precautions

Proper electrostatic discharge (ESD) precautions should be observed at all times when handling the DSK_COMM4 daughtercard. Failure to do so may result in damage to the circuitry on the daughtercard or the DSK. Do not install or remove the daughtercard while power is supplied to the DSK.

1.3 Installation

Installation should only be accomplished in an ESD-safe area. Disconnect all power to the DSK. Install the DSK_COMM4 daughtercard on the DSK's Peripheral Interface and External Memory Interface connectors. Pay careful attention to the pin 1 keying on the connectors.

IMPORTANT: Before connecting the daughtercard USB connector to a computer, you must install the FTDI USB drivers on the computer. The USB drivers are linked on the Educational DSP web page.

1.4 Daughtercard Memory Map and Decoding

The DSK_COMM4 serial ports, CPLD, and other resources are mapped into memory as shown below. The address offsets shown are based on byte-wide EMIF operation. The UART channels each decode eight distinct internal register locations with the range shown. The CPLD registers are partially decoded, so a given CPLD register can be accessed at any address within its specified range. The appropriate base address and register offsets for each supported DSK are automatically calculated by the *dsk_comm4_xxxx.h* files included in the sample software projects. These files also include bit definitions for the CPLD registers.

Offset Range[1]	Mapping
0x00-0x07	UART channel A
0x08-0x0F	UART channel B
0x10-0x17	UART channel C
0x18-0x1F	UART channel D
0x20-0x27	CPLD_INTRT: Interrupt routing (write) CPLD_STATUS: Status (read)
0x28-0x2F	CPLD_INTCNF: Interrupt polarity/driver configuration and USB interrupt routing (write)
0x30-0x37	CPLD_DIGOUT: Digital output (write) CPLD_DIGIN: Digital input (read)
0x38-0x3F	CPLD_USB: USB FIFO data (read/write)

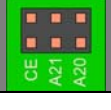
Notes:

1. For the 5510 DSK, multiply all offsets by 2. (The 5510 DSK does not use A1:0, and all 5510 addresses are word addresses.)

Detailed information on the UART's internal organization, operation, and registers can be obtained from the TL16C554 datasheet available on the Educational DSP website. The CPLD register organization is shown in detail in section 1.5.

1.4.1 Base Memory Address Selection Jumpers

The base memory address of the DSK_COMM4 can be changed by placing/removing shunts on the JP1 header. The table below lists the base address for all jumper combinations and DSK types. The board is shipped with all three jumpers installed. The highest base address is obtained when no jumpers are installed. The header file in the sample CCS projects assumes that all three jumpers are installed. To change the base address, remove the desired jumpers and then comment out the corresponding lines in the header file.

JP1 settings	5510/5509[1]	5416[2]	6xxx[3]
	0x400000 (CE2 space)	0x8000 (PGM=0x00)	0xA0000000 (CE2 space)
	0x480000 (CE2 space)	0x8000 (PGM=0x08)	0xA0040000 (CE2 space)
	0x500000 (CE2 space)	0x8000 (PGM=0x10)	0xA0080000 (CE2 space)
	0x580000 (CE2 space)	0x8000 (PGM=0x18)	0xA00C0000 (CE2 space)
	0x600000 (CE3 space)	Not supported	0xB0000000 (CE3 space)
	0x680000 (CE3 space)	Not supported	0xB0040000 (CE3 space)
	0x700000 (CE3 space)	Not supported	0xB0080000 (CE3 space)
	0x780000 (CE3 space)	Not supported	0xB00C0000 (CE3 space)

Notes:

1. Addresses for the 5510/5509 are word addresses.
2. Addresses for the 5416 are data space addresses.
3. The 6xxx EMIF is operated in 8-bit asynchronous mode.

The recommended EMIF configuration for each type of DSK is shown below. The registers for the appropriate memory space must be configured, depending on the setting of the JP1 CE jumper.

DSK	Recommended EMIF Configuration
5416	SWWSR = 0x2E49, BSCR = 0xA806, SWCR = 0x0001 (assumes CLKMD1 off, CLKMD2-3 on)
5509/5510	CEn1 = 0x1443, CEn2 = 0x543B, CEn3 = 0x0000 (assumes 200MHz CPU clock)
6211/6711	TBD
6416T	CEn = 0x3333CE0F (assumes 125MHz EMIFA clock)
6713	CEn = 0x21F2C804 (assumes 100MHz EMIF clock)

Note that for the 6416T DSK, care must be taken that the daughtercard is not written to too quickly under certain conditions. This is a particular concern during UART configuration and when reading/writing in FIFO mode. (I.e., in FIFO mode, you must allow 425ns (min) between reads of the receiver FIFO and the status registers (interrupt-identification register and line-status register). See the TL16C554 datasheet for further details.

1.5 CPLD Register Definitions

The binary values shown for each of the CPLD registers are the initial values after a daughtercard reset.

CPLD_INTRT: Interrupt routing (write-only)

The CPLD_INTRT register is used to determine the routing of the four individual UART interrupts. Multiple UART channels can be mapped to the same DSK interrupt request line. Each UART interrupt can be mapped to the following;

0 – DSK interrupt 0 (INT0)
1 – DSK interrupt 1 (INT1)
2 – DSK interrupt 2 (INT2)
3 – DSK interrupt 3 (INT3)

See section 1.4 for DSK specific interrupt pin assignments.

D7	D6	D5	D4	D3	D2	D1	D0
INTD_destination		INTC_destination		INTB_destination		INTA_destination	
11		10		01		00	

CPLD_STATUS: Status (read-only)

The CPLD_STATUS register reports the state of the current interrupt polarity and drive settings, the USB FIFO status, and the UART channel interrupt request lines.
INT_OD – a 1 indicates open-drain drivers are in use.
INT_INV – a 1 indicates active-low interrupts in use.
USB_TXF# – a 1 indicates that the USB FIFO should not be written to.
USB_RXE# – a 1 indicates that the USB FIFO should not be read from.
INTD – a 1 indicates UART channel D has an active interrupt request
INTC – a 1 indicates UART channel C has an active interrupt request
INTB – a 1 indicates UART channel B has an active interrupt request
INTA – a 1 indicates UART channel A has an active interrupt request

D7	D6	D5	D4	D3	D2	D1	D0
INT_OD	INT_INV	USB_TXF#	USB_RXE#	INTD	INTC	INTB	INTA

CPLD_INTCNF: Interrupt polarity and driver configuration (write-only)

The CPLD_INTCNF register is used to configure the interrupt polarity and driver configuration, and to set/disable the interrupt request routing assigned to the USB FIFO interrupt.
INT_OD – set to 1 to use open-drain drivers on the interrupt request lines to the DSK.
INT_INV – set to 1 to invert the active-high UART interrupts.
USB_INTDIS – set to 1 to disable interrupt generation for the USB FIFO
USB_INTRT – set to the desired interrupt routing for the USB FIFO interrupt

D7	D6	D5	D4	D3	D2	D1	D0
INT_OD	INT_INV	ignored	ignored	ignored	USB_INTDIS	USB_INTRT	
1	1	X	X	X	1	11	

CPLD_DIGOUT: Digital output (write-only) **CPLD_DIGIN: Digital input (read-only)**							
The CPLD_DIGOUT/CPLD_DIGIN registers are used to access the digital inputs and digital outputs on the daughtercard. Writes to CPLD_DIGOUT set the value on the DOUT[7:0] pins. On reset, the digital outputs are set to 1. Reads from CPLD_DIGIN will return the value of the DIN[7:0] pins. Unconnected DIN[7:0] pins will read 0.							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
DOUT7/DIN7	DOUT6/DIN6	DOUT5/DIN5	DOUT4/DIN4	DOUT3/DIN3	DOUT2/DIN2	DOUT1/DIN1	DOUT0/DIN0

CPLD_USB: USB FIFO data (read/write)							
The CPLD_USB register is used to transfer data to and from the USB FIFO device.							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
USB-D7	USB-D6	USB-D5	USB-D4	USB-D3	USB-D2	USB-D1	USB-D0

1.6 Daughtercard Interrupts

The interrupt signals from each UART channel and the USB FIFO can each be routed to any of the four interrupt request lines on the DSK. In the reset configuration, the interrupts are inverted to active-low and are driven with totem-pole outputs. The CPLD_INTCNF register permits selecting active-high interrupts and open-drain drivers. The *dsk_comm4_xxxx.h* files included in the sample software projects include DSK-specific definitions for each of the routing destinations.

	CPLD_INTRT destination field value			
DSK	0	1	2	3
5416	XINT0 (DSK P2-53)	XINT1 (DSK P2-48)	XINT2 (DSK P2-67)	XINT3 (SINT8) (DSK P2-68)
5510/5509A	X_INT1n (SINT16) (DSK P2-53)	X_INT2n (SINT3) (DSK P2-48)	X_INT3n (SINT11) (DSK P2-67)	X_INT0n (SINT2) (DSK P2-47)
6211/6711	EINT4 (DSK J3-53)	EINT5 (DSK J3-48)	EINT6 (DSK J3-67)	EINT7 (DSK J3-68)
6416	EINT4 (DSK J3-53)	EINT5 (DSK J3-48)	EINT6 (DSK J3-67)	EINT7 (DSK J3-68)
6713	EINT4 (DSK J3-53)	EINT5 (DSK J3-48)	EINT6 (DSK J3-67)	EINT7 (DSK J3-68)

1.7 Baud Rate Selection

The TL16C554A quad UART operates with a master clock of 14.7456MHz. The UARTs use 16x oversampling, so the baud rate is given by $f_{baud} = \frac{14.7456MHz}{16 \cdot DL}$, where DL is the value set in the UART baud rate generator registers DLM:DLL. The baud rate divisor register settings for a number of standard baud rates are shown below.

Baud Rate	DL	DLM	DLL
300	3072	0x0C	0x00
2400	384	0x01	0x80
9600	96	0x00	0x60
38.4k	24	0x00	0x18
115.2k	8	0x00	0x08
230.4k	4	0x00	0x04
921.6k	1	0x00	0x01

The *dsk_comm4_xxxx.h* files included in the sample software projects include definitions for standard baud rates.The RS232 level translators are specified to operate at up to 250kbaud. The RS422 transceivers are specified to operate at all possible UART baud rates.

1.8 Digital Input/Output

The digital input and output pins are implemented directly in the CPLD. The state of the output pins is set by a write to the CPLD_DIGOUT register. The digital outputs are 3.3V logic, with a maximum current rating of 25mA per pin. Reading the CPLD_DIGOUT register returns the state of the input pins. The digital inputs are 3.3V logic, but will tolerate input voltages up to 5V. See the Altera MAX3000 series documentation for further information on the CPLD pin capabilities.

Note that the digital inputs and outputs do not have any protection circuitry. If the user cannot be certain that the current and voltage requirements of the MAX3000 will be met, or if electrostatic discharge hazards exist, external circuitry should be added to protect the CPLD pins.

1.9 Serial Interface Connector Pin-Outs

The RS232 interface is implemented as a full Data Terminal Equipment (DTE) interface including all modem control signals. The RS422 interface is implemented as a full-duplex transceiver. UART A and B are always configured as RS232. UART C and/or D can be configured at the factory as either RS232 or RS422. A male 9-pin D-subminiature (DB9) connector is used for all connections. The connector pin-outs are shown below.

Pin	RS232	RS422
1	DCD	RXD-
2	RXD	TXD+
3	TXD	TXD-
4	DTR	-
5	Ground	Ground
6	DSR	-
7	RTS	-
8	CTS	-
9	RI	RXD+

1.10 USB FIFO

The USB FIFO is implemented with an FTDI FT245RL device. The “USB” LED on the daughtercard illuminates when the USB interface has connected to a host computer. The transmit and receive FIFO status bits can be read in the CPLD_STATUS register. The CPLD can also generate an interrupt when external data is received by the USB FIFO (i.e. when the receive FIFO goes from empty to non-empty). The CPLD_INTCNF register can be used to enable/disable the interrupt generation, as well as to route the generated interrupt to any of the four DSK interrupt signals. See the Educational DSP website for further information on the FT245R device and for USB driver downloads.

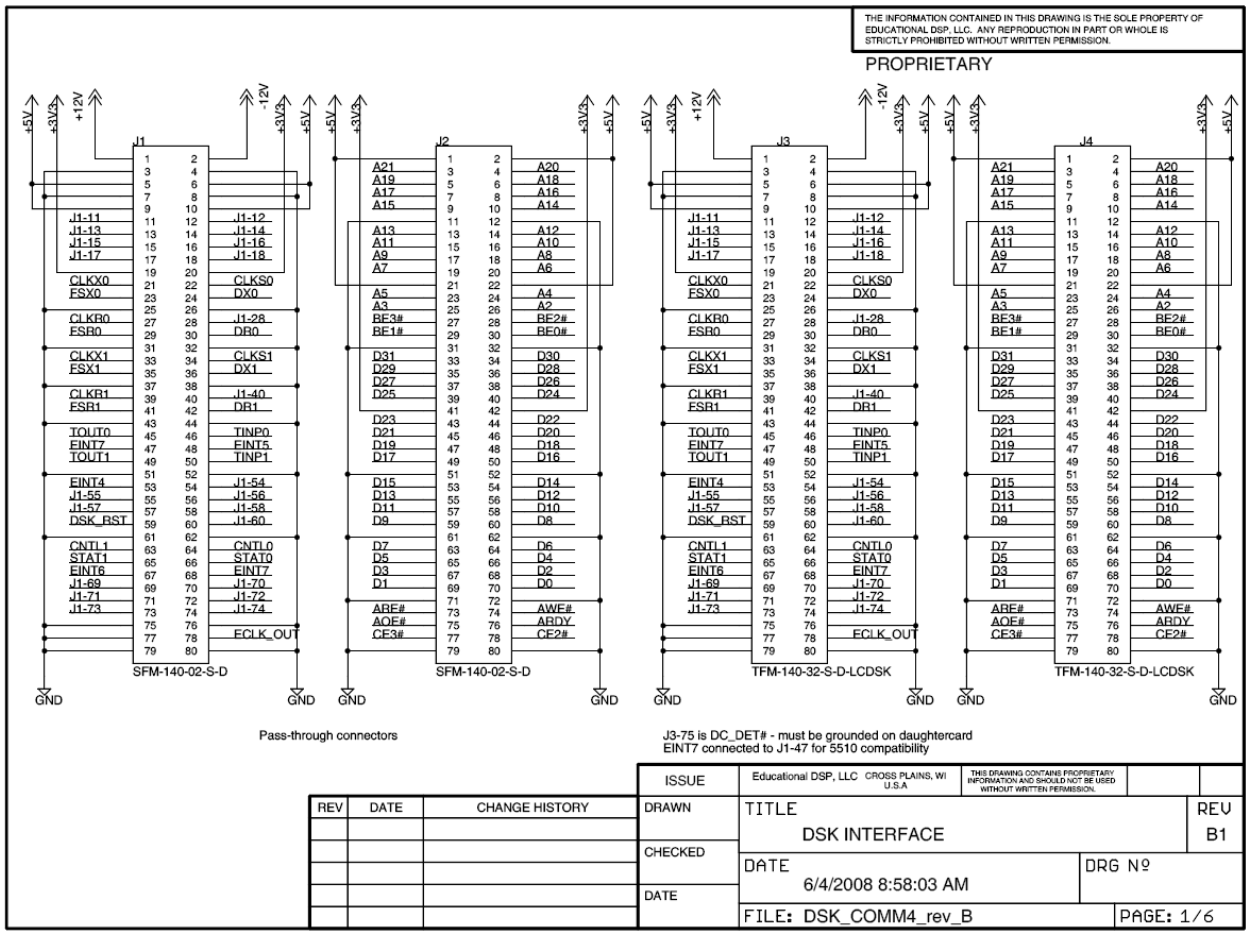
1.11 XBee Radio Module

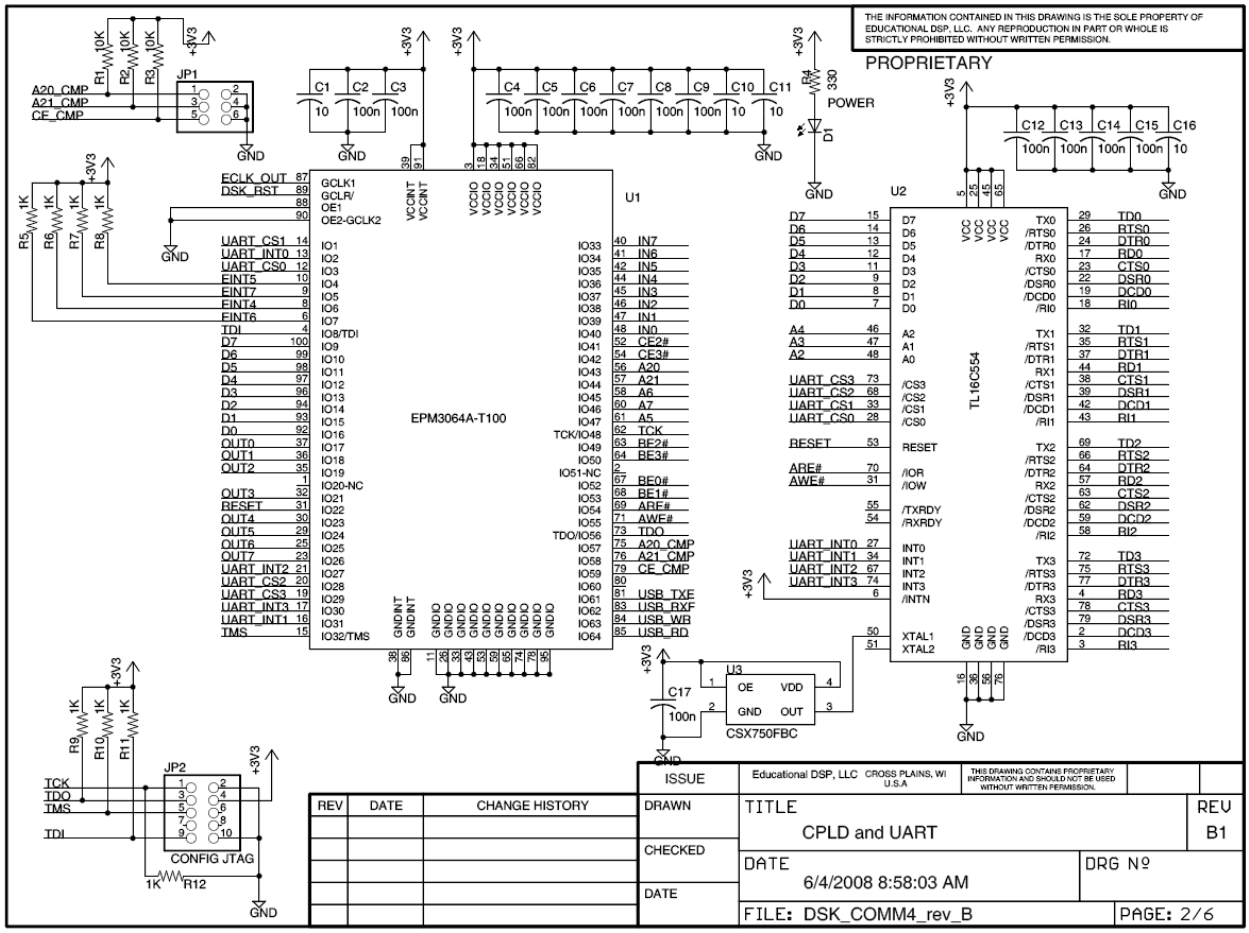
UART C and/or D can be configured at the factory with a Digi (MaxStream) XBee 2.4GHz radio module instead of a wired connection. See the XBee series documentation on the Educational DSP website for further information.

2 Sample Software Applications

Complete Code Composer Studio (CCS) sample software projects are available on the Educational DSP website for each supported DSK. Each project includes a detailed header file specific to the DSK to make coding easier. The software in the project performs loopback testing of the base RS-232 channels, the optional UART channels, the USB interface, and digital input/output. These projects provide an excellent base for developing user applications.

3 Schematic Diagrams

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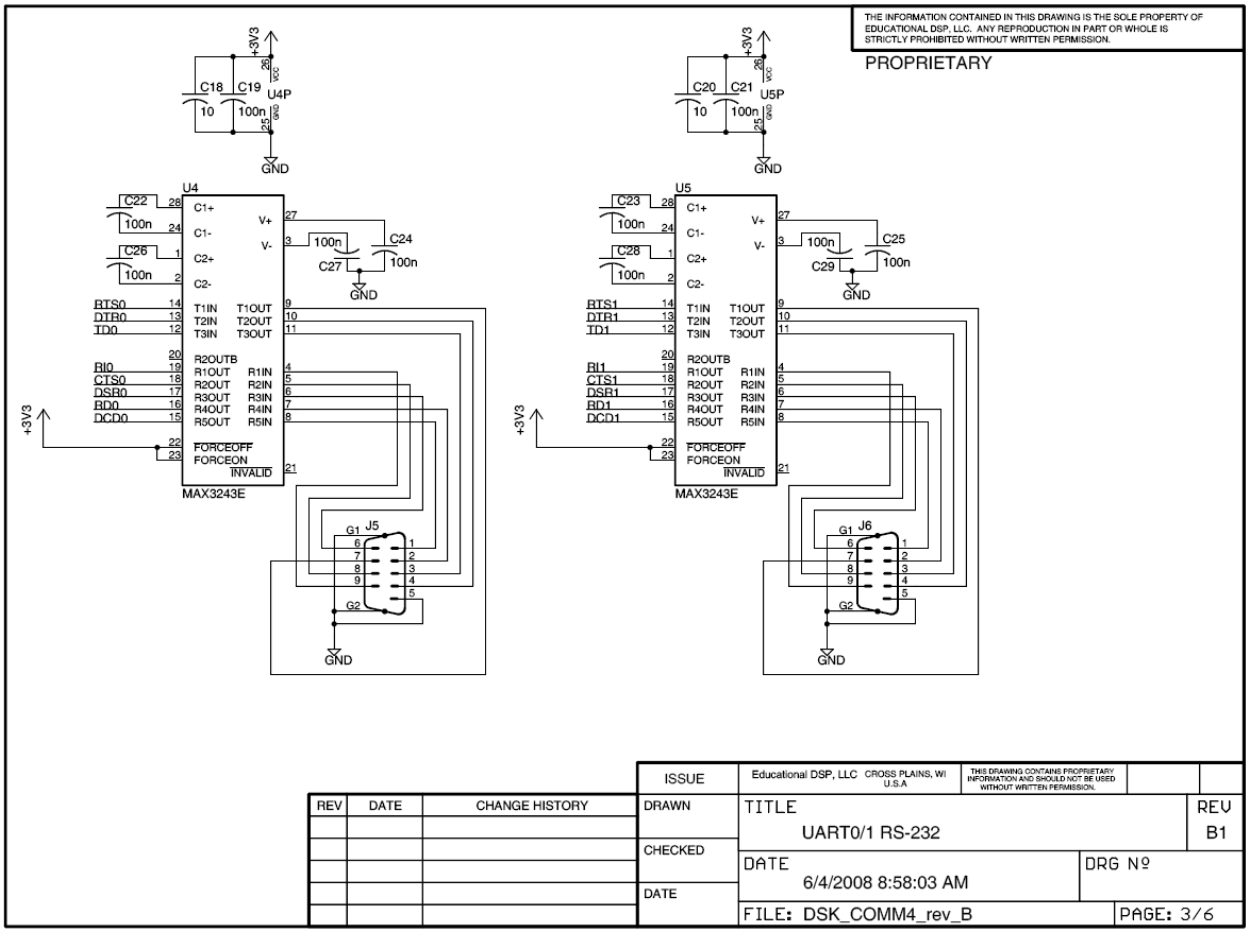
PROPRIETARY
EPM3064A-T100
TL16C554
CSX750FBC
CONFIG JTAG
POWER
Educational DSP, LLC CROSS PLAINS, WI U.S.A
THIS DRAWING CONTAINS PROPRIETARY INFORMATION AND SHOULD NOT BE USED WITHOUT WRITTEN PERMISSION.
REV
DATE
CHANGE HISTORY
ISSUE
DRAWN
CHECKED
DATE
TITLE
CPLD and UART
REV
B1
DATE
6/4/2008 8:58:03 AM
DRG Nº
FILE: DSK_COMM4_rev_B
PAGE: 2/6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PROPRIETARY
+3V3
C18 C19 U4P
10 100n
GND
U4
C22 100n
C26 100n
C24 100n
C27 100n
RTS0 DTR0 TD0
RI0 CTS0 DSR0 BD0 DCD0
T1IN T2IN T3IN
T1OUT T2OUT T3OUT
R2OUTB
R1OUT R2OUT R3OUT R4OUT R5OUT
R1IN R2IN R3IN R4IN R5IN
FORCEOFF
FORCEON
INVALID
MAX3243E
J5
C20 C21 U5P
C23 C25 C28 C29
RTS1 DTR1 TD1
RI1 CTS1 DSR1 BD1 DCD1
U5
J6
ISSUE
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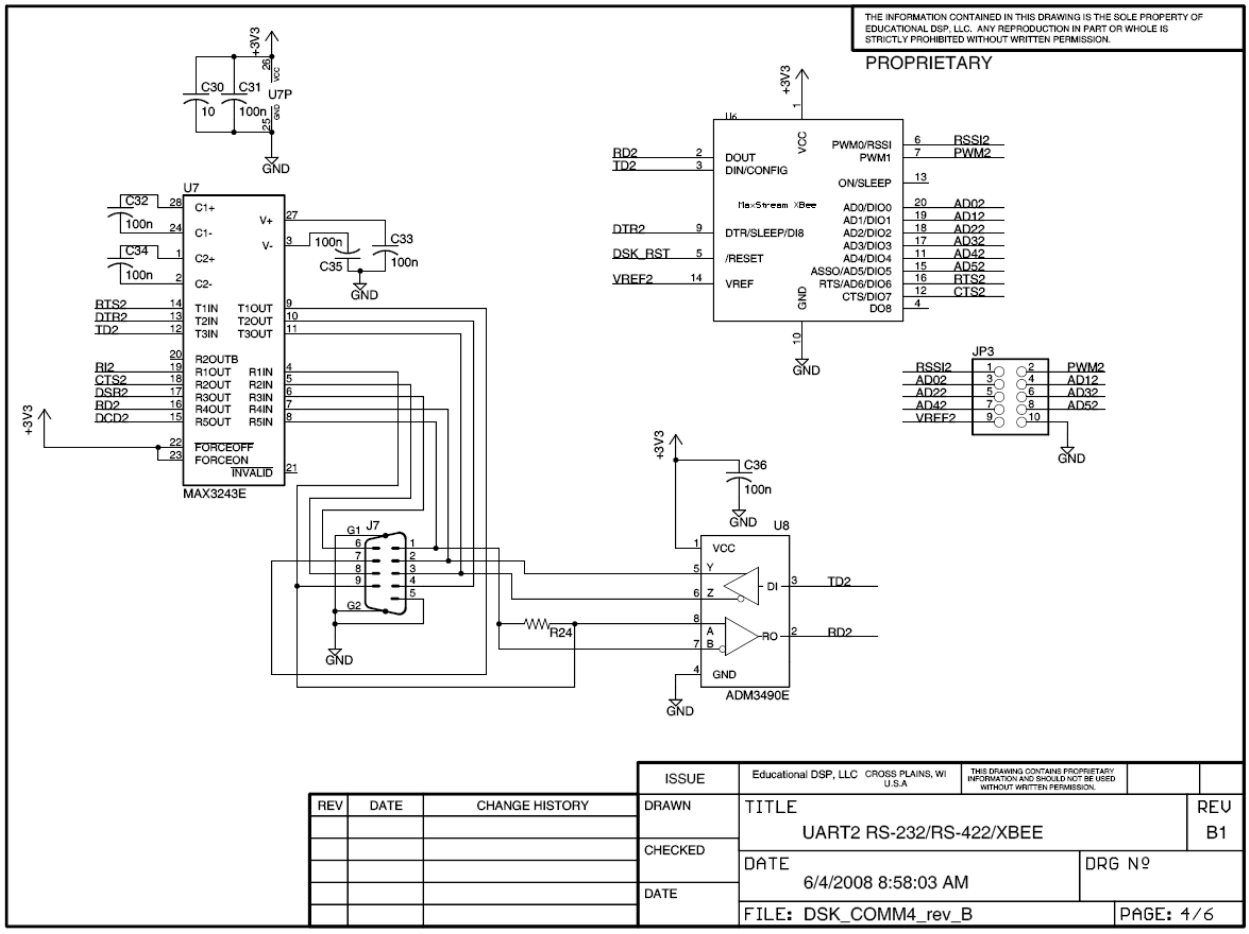
THIS DRAWING CONTAINS PROPRIETARY INFORMATION AND SHOULD NOT BE USED WITHOUT WRITTEN PERMISSION.
REV DATE CHANGE HISTORY
DRAWN
CHECKED
DATE
TITLE
UART0/1 RS-232
REV
B1
DATE
6/4/2008 8:58:03 AM
DRG Nº
FILE: DSK_COMM4_rev_B
PAGE: 3/6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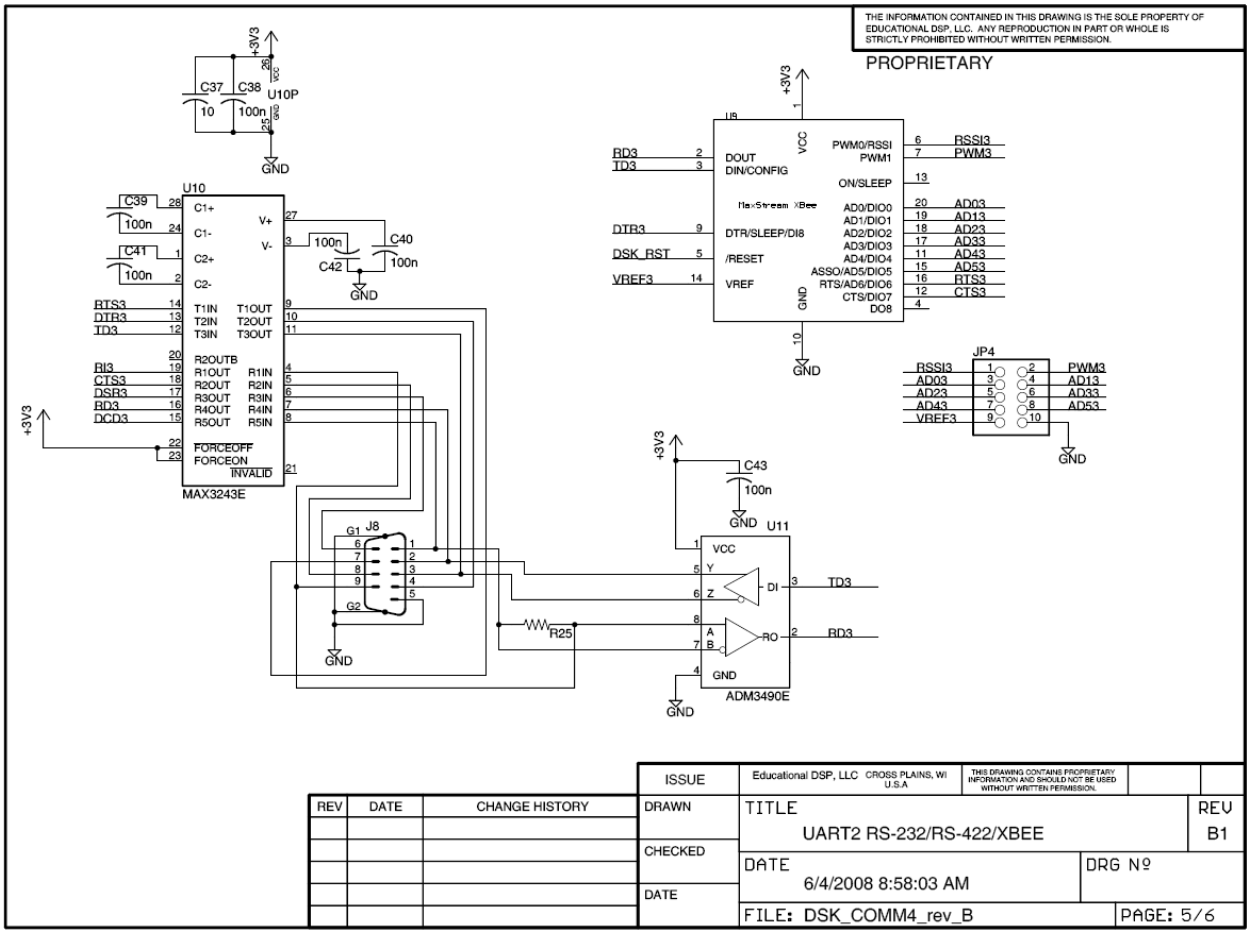
PROPRIETARY
U7P
C30
C31
10
100n
+3V3
GND
U7
MAX3243E
C32
C33
C34
C35
100n
RTS2
DTR2
TD2
RI2
CTS2
DSR2
RD2
DCD2
FORCEOFF
FORCEON
INVALID
J7
G1
G2
R24
U6
DOUT
DIN/CONFIG
DTR/SLEEP/DI8
/RESET
VREF
VCC
PWM0/RSSI
PWM1
ON/SLEEP
AD0/DIO0
AD1/DIO1
AD2/DIO2
AD3/DIO3
AD4/DIO4
ASSO/AD5/DIO5
RTS/AD6/DIO6
CTS/DIO7
DO8
RD2
TD2
DTR2
DSK_RST
VREF2
RSSI2
PWM2
AD02
AD12
AD22
AD32
AD42
AD52
RTS2
CTS2
JP3
C36
U8
ADM3490E
VCC
Y
Z
DI
RO
A
B
TD2
RD2
ISSUE
REV
DATE
CHANGE HISTORY
DRAWN
CHECKED
DATE
Educational DSP, LLC CROSS PLAINS, WI U.S.A
THIS DRAWING CONTAINS PROPRIETARY INFORMATION AND SHOULD NOT BE USED WITHOUT WRITTEN PERMISSION.
TITLE
UART2 RS-232/RS-422/XBEE
REV
B1
DATE
6/4/2008 8:58:03 AM
DRG Nº
FILE: DSK_COMM4_rev_B
PAGE: 4/6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PROPRIETARY
U10P
C37 10
C38 100n
+3V3
GND
U10
MAX3243E
C39 100n
C40 100n
C41 100n
C42 100n
RTS3
DTR3
TD3
RI3
CTS3
DSR3
RD3
DCD3
T1IN T1OUT
T2IN T2OUT
T3IN T3OUT
R1OUT R1IN
R2OUT R2IN
R3OUT R3IN
R4OUT R4IN
R5OUT R5IN
FORCEOFF
FORCEON
INVALID
U9
MaxStream XBee
DOUT
DIN/CONFIG
DTR/SLEEP/DI8
/RESET
VREF
VCC
GND
PWM0/RSSI
PWM1
ON/SLEEP
AD0/DIO0
AD1/DIO1
AD2/DIO2
AD3/DIO3
AD4/DIO4
ASSO/AD5/DIO5
RTS/AD6/DIO6
CTS/DIO7
DO8
RD3
TD3
DTR3
DSK_RST
VREF3
RSSI3
PWM3
AD03
AD13
AD23
AD33
AD43
AD53
RTS3
CTS3
JP4
J8
G1
G2
R25
C43 100n
U11
ADM3490E
VCC
Y
Z
A
B
DI
RO
GND
TD3
RD3
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REV DATE CHANGE HISTORY
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CHECKED
DATE
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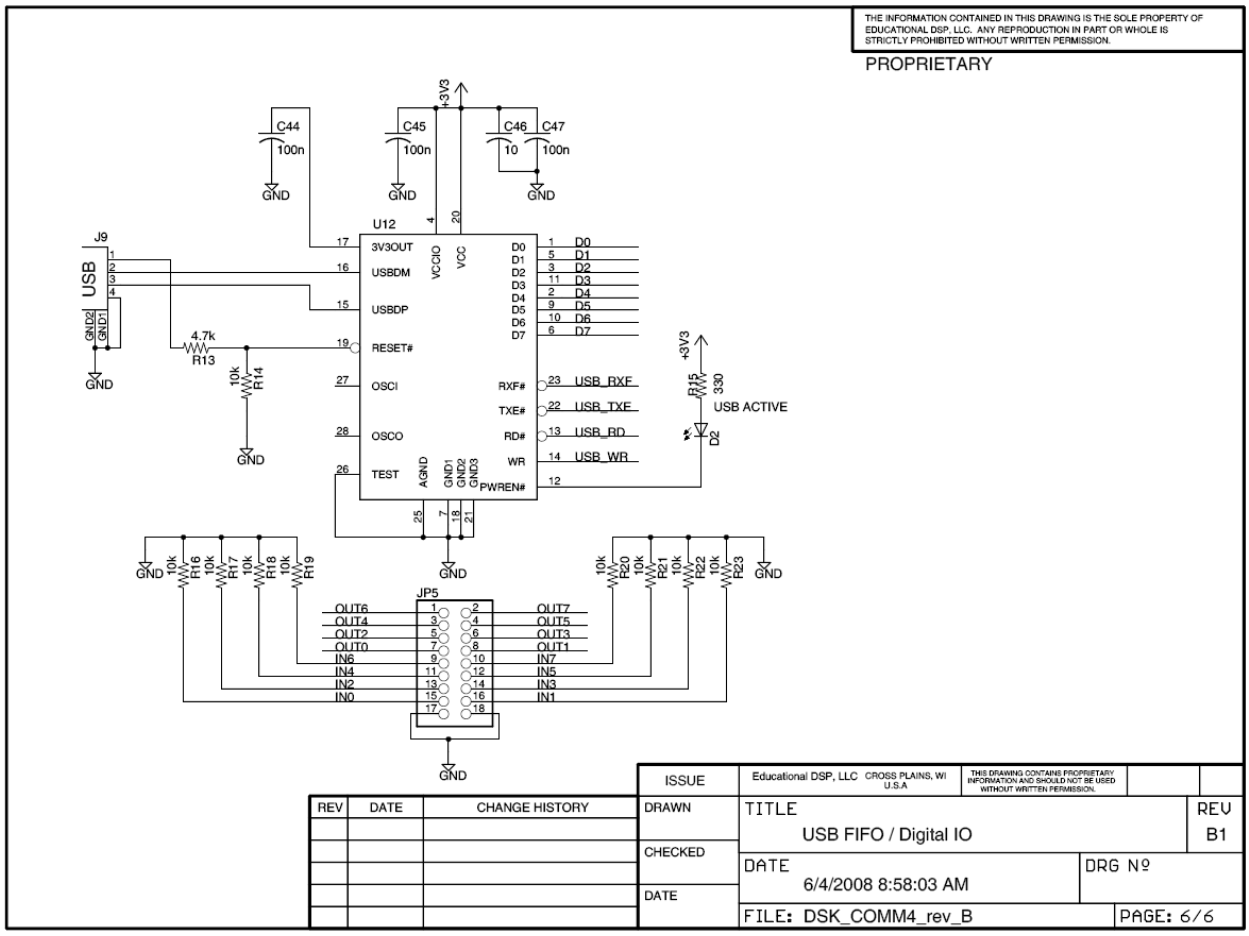
TITLE
UART2 RS-232/RS-422/XBEE
REV
B1
DATE
6/4/2008 8:58:03 AM
DRG Nº
FILE: DSK_COMM4_rev_B
PAGE: 5/6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PROPRIETARY
U12
J9
USB
JP5
USB ACTIVE
ISSUE
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REV
DATE
CHANGE HISTORY
DRAWN
CHECKED
DATE
TITLE
USB FIFO / Digital IO
REV
B1
DATE
6/4/2008 8:58:03 AM
DRG Nº
FILE: DSK_COMM4_rev_B
PAGE: 6/6

4 Board Layout